High-Density High-Speed Holographic Memory

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Abstract - An innovative holographic memory system has been developed at JPL for high-density and high-speed data storage in a space environment. This system utilizes a newly developed electro-optic (E-O) beam steering technology to achieve a design goal of up to 250 Gb storage in a cubic photorefractive crystal with up to 1 Gb/sec transfer rate. Recently, a compact CD-sized holographic memory breadboard has been developed and demonstrated for holographic data storage and retrieval. Detail technical progress will be presented in this paper.

I. INTRODUCTION

JPL is currently developing a new holographic memory system with performance characteristics including: read/rewrite capability, high-density, high transfer rate, non-volatility, compactness, and radiation resistance. These characteristics are selected to meet requirements for data storage needs for both NASA's space missions and commercial applications.

NASA's future missions would require massive high-speed onboard data storage capability to support Earth Science missions. With regard to Earth science observation, a 1999 joint Jet Propulsion Laboratory and Goddard Space Flight Center (GFSC) study ("The High Data Rate Instrument Study") has pointed out that the onboard science data (collected by high date rate instruments such as hyperspectral and synthetic aperture radar) stored between downlinks would be up to 40 terabits (Tb) by 2003. However, onboard storage capability in 2003 is estimated at only 4 Tb that is only 10% of the requirement. By 2006, the storage capability would fall further behind that would only be able to support 1% of the onboard storage requirements.

Current technology, as driven by the personal computer and commercial electronics market, is focusing on the development of various incarnations of Static Random Access Memory (SRAM), Dynamic Random Access Memory (DRAM), and Flash memories. Both DRAM and SRAM are volatile. Their densities are approaching 256 Mbits per die. Advanced 3-D multichip module (MCM) packaging technology has been used to develop solid-state recorder (SSR) with storage capacity of up to 100 Gbs [3]. The Flash memory, being non-volatile, is rapidly gaining popularity. Densities of flash memory of 256 Mbits per die exist today. High density SSR could also be developed using the 3-D MCM technology. However, Flash memory is presently faced with two insurmountable limitations: Limited endurance (breakdown after repeated read/write cycles) and poor radiation-resistance (due to simplification in power circuitry for ultra-high density package).

It is obvious that state-oft-the-art electronic memory could not satisfy all NASA mission needs. It has motivated JPL to develop new memory technology that would simultaneously satisfy non-volatility, rad-hard, long endurance as well as high density, high transfer rate, low power, mass and volume to meet all NASA mission needs.

II. COMPACT HOLOGRAPHIC MEMORY USING ELECTRO-OPTIC BEAM STEERING

The holographic memory architecture is shown in Figure 1. Collimated laser beam first enters PBS_1 (polarizing beam splitter 1) and on exit, is split into two beams. The input beam subsequently passes through the data SLM (spatial light modulator), L_3 (lens 3) – M_1 (mirror 1) – M_2 – M_3 – L_4 and then reaches the PRC (a Fe:$LiNbO_3$ photorefractive crystal). The lens pair L_3 – L_4 will relay the data SLM throughput image onto the PRC, the mirror set M_1 – M_2 – M_3 will fold and increase the light path length to make it equal to that of the reference beam. The reference beam, after exiting PBS_1, will subsequently pass through L_3 – PBS_2, -$BSSLM_1$ (Beam Steering SLM 1) - PBS_2 - L_3 – PBS_3 -$BSSLM_1$ – PBS_3 – L_4 and then reach the PRC. The data beam and the reference beam intersect within the volume of the PRC forming a 90^o recording geometry. Both beams are polarized in the direction perpendicular to the incident plane (the plane formed by the reference and signal beams). L_3 – L_4 is a lens pair to relay the $BSSLM_1$ onto the PRC surface. BSSLM1 will scan the reference beam along the horizontal plane (or the x-axis) in parallel with the C-axis. $BSSLM_2$ will steer the reference beam in the vertical plane (y-axis, or the fractal plane). During holographic data recording, the interference pattern formed by each page of input data beam and the specifically oriented reference beam will be recorded in the PR crystal. The reference beam angle (and location) will be altered with each subsequent page of input data. During readout, the data beam will be shut down and the reference beam will be activated to illuminate the PR crystal. Due to the principle of holographic wavefront reconstruction, the stored page data, corresponding to a specific reference beam angle, will be readout. The readout data beam will exit the PRC and pass through M_4 and L_5 before reaching the Photodetector (PD) Array. Note that the lens set L_3 – L_4 – L_5 will relay the input SLM to the PD array. The magnification factor, caused by the lens set, is determined by the aspect ratio between the data SLM and the PD array.

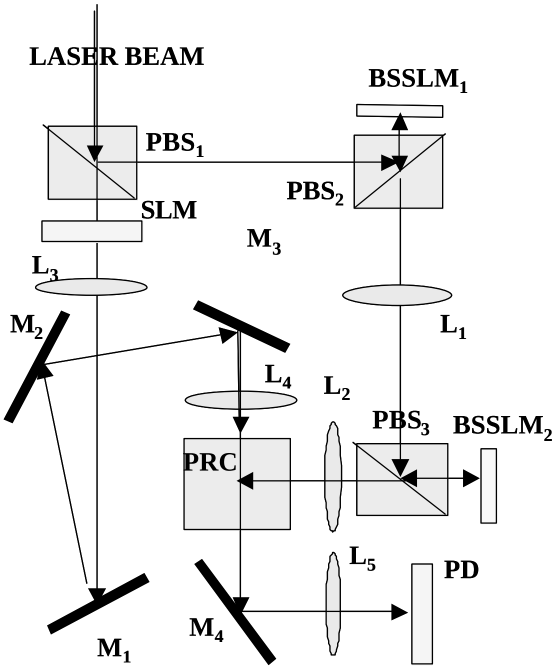

Figure 1. System architecture of compact holographic memory breading using a 2-D E-O angular-fractal multiplexing beam steering technology.

A. 2-D Angular-Fractal Multiplexing Scheme

As depicted in Figure 1, by using two 1-D BSSLMs cascaded in an orthogonal configuration, a 2-dimensional angular-fractal multiplexing scheme has been formed, for the first time, in a JPL developed breadboard setup to enable the high-density recording and retrieval of holographic data.

In experiments, holograms were first multiplexed with x-direction (in-plane) angle changes while y direction angle holds unchanged. After finish the recording of a row of holograms, we then changed the y direction (perpendicular to the incident plane) angle, and recorded the next row of holograms with x-direction angle changes. Both x and y angle changes are fully computer controlled and can be randomly accessed. Currently we have successfully performed the recording and retrieval of long video clips of high quality holograms using this compact breadboard.

Unique advantages of this E-O beam steering scheme include: absence of mechanical motion, high-transfer rate (1Gb/sec), random access data addressing, low-volume and low power.

B. Beam Steering Spatial Light Modulator

The BSSLM used in out experimental investigation has been custom developed by the Boulder Nonlinear System Inc. (BNS) for JPL This device is built upon a VLSI back plane in ceramic PGA carrier. A 1-dimensional array of 4096 pixels, filled with Nematic Twist Liquid Crystal (NTLC), is developed on the SLM surface. The device aperture is of the size of 7.4 μm x 7.4 μm, each pixel is of 1.8 μm x 7.4 μm in dimension.

The principle of operation of this BSSLM is illustrated in Figure 2. Since the SLM is a phase-modulation device, by applying proper addressing signals, the optical phase profile (i.e. a quantized multiple-level phase grating) would repeats over a 0-to-2π) ramp with a period d. The deflection angle q of the reflected beam will be inversely proportional to d:

$$q = \sin^{-1}\left(l/d \right)$$

Where λ is the wavelength of the laser beam. Thus, beam steering can be achieved by varying the period of the phase grating

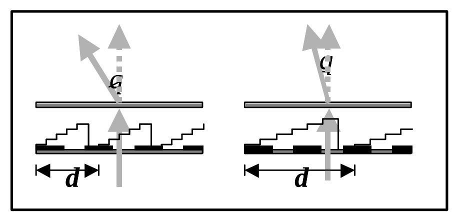

Figure 2. Beam steering using a phase modulation SLM with variable grating period.

For example, if each period d consists of 8 phase steps each with 1.8 μm pixel pitch. The period d will be 14.4 μm. With the operating wavelength at 0.5 μm, the total beam steering angle will be about +/- 3.2^o . The total angle of diffraction will be 6.4^o. In the next development step, the pixel pitch can be reduced by 0.5 μm and the corresponding total beam steering angle will be increased to 22.5^o.

The Number of resolvable angles of the steered beam can be defined by:

$$M = 2m/n + 1$$

Where *m* is the pixel number in a subarray, and *n* is the minimum number of phase steps used. For example, the number resolvable angle M of a 4096 array (i.e. m = 4096) with of 8 phase levels (i.e. n = 8) would be 910. The current device is configured into eight 1 x 512 subarray due to the resolution limits of the foundry process. Therefore there are only 129 resolvable angles are available for the BSSLM used in our experimental setup. A photo of the liquid crystal BSSLM used in our experimental set up is shown in Figure 3.

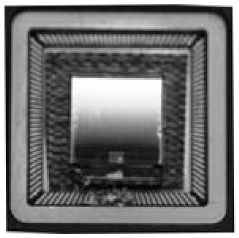

Figure 3. A photo of the LC BSSLM.

We have developed a custom phase-array profile driver and use a LabView based system HW/SW controller for the downloading of this driving profile to the BSSLM. Figure 4(a) shows the driving voltage profile used to achieve a very high diffraction efficiency (> 80%) for the steered beam. A sample of beam steering trace is shown in 4(b).

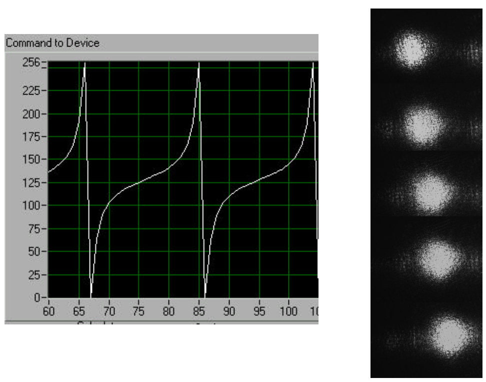

Figure 4. (a) BSSLM voltage driving waveform for high-efficiency beam steering using the LabView controller. (b) An example of the steered beam trace recorded using the BSSLM.

C. Holographic Memory Storage Capacity and transfer rate

The current 1 x 4096 array aperture size is 7.4 mm x 7.4 mm. In near future, the array size can be expanded to 2.5 mm x 2.5 mm (1 in^2) and the corresponding array density would be 1 x 12000. The number of resolvable angle would in terms be increased to 2666.

From the above analysis, it is clear that the Liquid Crystal BSSLM utilized in our holographic memory setup is appropriate for high-density holographic storage. With the follow-on upgrading in BSSLM performance currently underway, the total number of the holograms that can be recorded in our holographic memory breadboard would easily exceed 20,000. This could be configured by recording 2000 holograms in each x-dimension row (i.e. the angular direction) and 10 rows in y-dimension (i.e. the fractal direction).

The storage capacity of this holographic memory system, with using the upgraded E-O BSSLM, would then exceed 20 Gb for a 1000 pixel x 1000-pixel input page. It would further increase to 500 Gb by using a 5000 pixel x 5000 pixel input page. Further miniaturization would make enable the reduction of the holographic memory into a 5 cm x 5 cm x 1 cm cube. By stacking a multiple of such holographic memory cubes on a memory card (e.g. 10 x 10 cubes on each card) will achieve a storage capacity of 2 – 50 Tb per card. The transfer rate of this HM system will range from 200 Mb/sec (200 pages/sec, with a 1 M pixel page) to 5Gb/sec (200 pages/sec, with a 25 M pixel page).

III. HOLOGRAPHIC MEMORY BREADBOARD DEVELOPMENT WITH 1-D AND 2-D E-O BEAM STEERING

A. Book-sized Proof-of-Principle 1-D Holographic Memory Breadboard

During the course of NASA ESTO AIST sponsored task development, JPL has first developed a proof-of-principle holographic memory breadboard. This breadboard, for the first time, demonstrated the feasibility of using the new BSSLM device for beam steering to meet the multiplexing needs during holographic data recording and retrieval. This system utilized a single BSSLM and demonstrated 1-D beam steering for angular multiplexing. A photo of this 1-D holographic memory breadboard is shown in Figure 5. The system measures 30 cm x 20 cm x 5 cm, the size of a phone book.

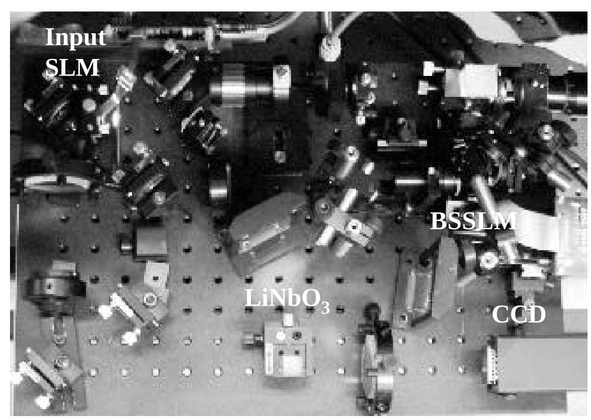

Figure 5. Photo of a JPL developed book-sized holographic memory breadboard, using 1-D E-O Beam Steering Technology, demonstrated during Phase I of the AIST sponsored task.

B. CD-Sized Compact Holographic Memory Breadboard with 2-D E-O Angular-Fractal Beam Steering

In FY 02, JPL has further miniaturized the book-size breadboard into a very compact CD-sized system. A photo of this breadboard is shown in Figure 6. The layout of this system follows the system schematic shown in Figure 1.

This CD-sized holographic memory breadboard, measuring 10 cm x 10 cm x 1 cm, is the most compact holographic memory module developed to date. The compact size of the VLSI based BSSLM together with advanced optics design has enabled the drastic reduction in the system volume from book-size to CD-size. This breadboard is capable of recording 10 Gb of holographic data. The current system design would make it possible the easy replacement of the key devices when a upgraded version becomes available. These key devices include the Spatial Light Modulator, the BSSLM, and the PD array. Moreover, the system storage capacity would be increased by up to 2 orders of magnitude (as described in Section II C). when the high-resolution BSSLM is developed.

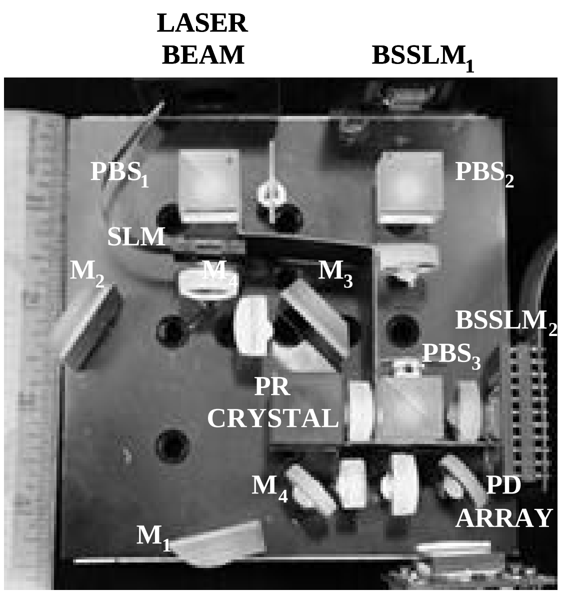

Figure 6. Photo of JPL Developed Compact Advanced Holographic Memory Breadboard of the size of a CD-sized (Volume of 10 cm x 10 cm x 2.5 cm, or 4” x 4” x 1”) using a 2-D E-O Beam Steering Technology with an Angular-Fractal Multiplexing Scheme.

C. Example of Holographically Recorded and Retrieved data

The CD-sized holographic memory breadboard has been developed with a comprehensive LabView based system controller. Hence autonomous data recording and retrieval would be available upon full integration of the system.
During the data storage test and evaluation, we have utilized the grayscale Toutatis Asteroid image sequence for benchmark testing. Some example of retrieved holographic images of the Toutatis asteroid, excerpted from a long recorded video clip, are shown in Figure 7.

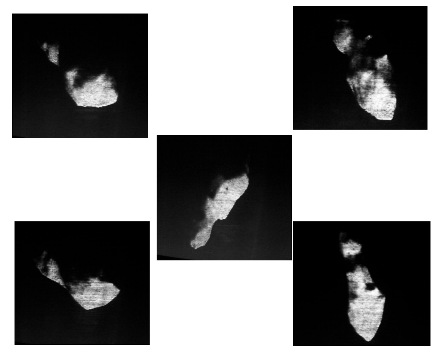

Figure 7. Example of retrieved holographic images of the Toutatis Asteroid.

IV. SUMMARY

JPL has successfully developed an advanced holographic memory technology to enable high-density and high-speed holographic data storage with random access during data recording and readout. An innovative E-O beam steering scheme, achieved by utilizing liquid crystal beam steering device, has been experimentally implemened. Recently, a CD-sized holographic memory breadboard has been integrated and demonstrated for successful holographic data recording and retrieval. This breadboard is the most compact one developed to date. It’s storage capacity ranges from 10 Gb to 250 Gb, depending on the input page size. With the completion of the next BSSLM upgrading and system integration, up to 2 orders of magnitude increase in storage capacity has been envisioned.

V. ACKNOWLEDGMENT

The research described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration.

VI. REFERENCE

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